IN THE CLAIMS

1. **(Currently Amended)** A semiconductor integrated circuit, comprising:

a ~~support~~ silicon substrate;

a ~~semiconductor~~ silicon layer that is formed on the ~~entire~~ surface of said ~~support~~ silicon substrate and has a lower resistivity than the resistivity of said ~~support~~ silicon substrate; ~~and~~

first and second circuit sections formed in ~~the semiconductor layer in an electrically isolated state from each other.~~ said silicon layer; and

a device isolation region projecting from said silicon substrate up to a surface of each of said first and second circuit sections between said first and second circuit sections.

2. **(Currently Amended)** The semiconductor integrated circuit according to Claim 1, wherein the resistivity of said ~~support~~ silicon substrate is 20 times or more the resistivity of said ~~semiconductor~~ silicon layer.

3. **(Currently Amended)** The semiconductor integrated circuit according to Claim 2, wherein the resistivity of said ~~support~~ silicon substrate is 50 times or more the resistivity of said ~~semiconductor~~ silicon layer.

4. **(Currently Amended)** The semiconductor integrated circuit according to Claim 1, wherein said ~~semiconductor~~ silicon layer is formed ~~on said support substrate by~~ of an epitaxial ~~growth.~~ layer.

5. **(Original)** The semiconductor integrated circuit according to Claim 1, wherein a digital circuit is formed on said first circuit section, and an analog circuit is formed on said second circuit section.

6. **(Currently Amended)** A ~~semiconductor substrate, where a first circuit section and a second circuit section are formed on the surface to compose a~~ semiconductor integrated circuit, ~~said substrate~~ comprising:

a ~~support~~ glass substrate; ~~and~~

a ~~semiconductor~~ silicon layer that is formed on the ~~entire~~ surface of ~~the support~~ said glass substrate, has a lower resistivity than the resistivity of said ~~support substrate, and where said~~ glass substrate;

first and second circuit sections ~~are electrically isolated from each other and~~ formed ~~in.~~ in said silicon layer; and

a device isolation region projecting from said glass substrate up to a surface of each of said first and second circuit sections between said first and second circuit sections.

7.-8. **(Cancelled).**

9. **(Currently Amended)** The semiconductor ~~substrate~~ integrated circuit according to Claim 6, wherein said ~~semiconductor~~ silicon layer is formed ~~on said support substrate by~~ of an epitaxial ~~growth.~~ layer.

10. **(Currently Amended)** The semiconductor ~~substrate~~ integrated circuit according to Claim 6, wherein a digital circuit is formed on said first circuit section, and an analog circuit is formed on said second circuit section.